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EXAMINER
LEE, CHRISTOPHER E

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19

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/540,676	CLINE, LESLIE E.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7-15 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-15 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 30th of March 2004. No claim has been amended; no claim has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 30th of December 2003. Currently, claims 1, 3-5, 7-15 and 17-21 are pending in this application.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 3-5, 7-11, 15 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. [US 6,131,134; hereinafter Huang] in view of Rafferty et al. [US 6,141,719 A; hereinafter Rafferty] and Pollard et al. [US 5,754,870 A; hereinafter Pollard].

Referring to claim 1, Huang discloses a method, comprising: providing a first resistor (pull-up resistor 340 of Fig. 3) with a first end (i.e., the end coupled to switch 330 in Fig. 3) and a second end (i.e., the end coupled to D+ in Fig. 3), said first end coupled to a switch (i.e., switch 330 of Fig. 3) and said second end coupled to a serial data bus wire (i.e., USB interface D+ of Fig. 3) at a near end of a serial data bus (i.e., detach control signal wire from converting circuit 310 to switch 330 and data lines D+ and D-, which are located within USB converter 120 in Fig. 3); controlling (i.e., opening or closing) said switch with a detach control signal (i.e., switch controlling signal from converting circuit 310 to switch 330 in Fig. 3) sent on a detach control signal wire (i.e., detach control signal wire) separate from data transmission wires (i.e., data lines D+ and D-) of said serial data bus (i.e., detach control signal wire and data lines D+, D-) to cause an apparatus (i.e., USB converter 120 of Fig. 3) containing said first resistor (i.e., resistor 340 of Fig. 3) and said switch (i.e., switch 330 of Fig. 3) to enter a logically detached state (See col. 6, lines 27-30 and 50-67; i.e., in fact, even if said apparatus is physically connected (i.e.,

physically attached), the open switch (e.g., no voltage is supplied to D+) makes said apparatus set said logically detached state); and switching (i.e., open or close said switch in Fig. 3) a biasing voltage (i.e., 3.3V in Fig. 3) from said resistor (i.e., resistor 340 of Fig. 3) utilizing said switch (i.e., switch 330 of Fig. 3).

Huang does not teach said logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus.

Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13-29) is sent from a far end (i.e., from a corresponding peripheral module; See col. 3, lines 26-28) of a serial data bus (i.e., bus 14 of Fig. 3; See col. 2, lines 43-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have received a logically detaching control signal from a far end of a serial data bus, as disclosed by Rafferty, in said apparatus, as disclosed by Huang, for the advantage of simulating insertion and removal (i.e., logically attaching and detaching) of said apparatus (i.e., USB device) by a corresponding far end device (i.e., a corresponding peripheral device; See Rafferty, col. 1, lines 50-58).

Huang, as modified by Rafferty, does not teach influencing said detach control signal with a wake-up signal sent on a wake-up signal wire separate from said data transmission wires of said serial data bus from said near end of said serial data bus to said far end of said serial data bus.

Pollard discloses a power management of a computer plug-in card having a remote data link 20 (Fig. 2), wherein influencing a detach control signal (i.e., command output 52 of Fig. 2) with a wake-up signal (i.e., 'link operable' signal 58 in Fig. 2) sent on a wake-up signal wire (i.e., status signal line 62 of Fig. 2) separate from a data transmission wires of a data bus (i.e., data bus with power source line 36 through connectors 26, 28 in Fig. 2) from a near end of said data bus (i.e., side of switch 46 in Fig. 2) to a far end of said data bus (i.e., side of host computer in Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said wake-up signal wire, as disclosed by Pollard, in said apparatus, as disclosed by Huang, as modified by Rafferty, so as said switch (i.e., power connect switch) to operate responsive to said wake-up signal (i.e., status signal) indicating the operability of said near end of said data bus (i.e., a status monitor indicative of the operability of the remote data link capability) from said near end (i.e., power-consuming elements on the card) to said far end (i.e., power source in the computer), which is disclosed at Pollard, col. 2, lines 43-48.

Huang, as modified by Rafferty and Pollard, teaches said method step of influencing said detach control signal (i.e., switch controlling signal from converting circuit 310 to switch 330 in Fig. 3; Huang) with said wake-up signal (i.e., 'link operable' signal 58 in Fig. 2; Pollard) sent on said wake-up signal wire (i.e., status signal line 62 of Fig. 2; Pollard) separate from said data transmission wires (i.e., data lines D+ and D- in Fig. 3; Huang) of said serial data bus (i.e., USB in Fig. 3; Huang) from said near end of said serial data bus (i.e., a side of switch) to said far end of said serial data bus (i.e., the other side of switch).

Referring to claim 3, Huang discloses said first resistor is configured as a pull-up resistor (pull-up resistor 340 of Fig. 3).

Referring to claim 4, Huang discloses detecting said switching of said biasing voltage (See col. 6, lines 30-35).

Referring to claim 5, Huang discloses determining a logically detached state responsive to said detecting (See col. 6, lines 28-30).

Referring to claim 8, Huang discloses an apparatus (i.e., USB converter 120 of Fig. 3), comprising: a first resistor with a first end and a second end (i.e., pull-up resistor 340 of Fig. 3); a switch (i.e., switch 330 of Fig. 3) coupled to said first end of said first resistor and a bias voltage (i.e., 3.3V in Fig. 3); a detach control signal wire (i.e., switch controlling signal arrow from converting circuit 310 to switch 330 in Fig. 3) separate from data transmission wires (i.e., data lines D+ and D-) of said serial data

bus (i.e., detach control signal wire and data lines D+, D-) coupled to said switch at a near end of a serial data bus (i.e., detach control signal wire from converting circuit 310 to switch 330 and data lines D+ and D-, which are located within USB converter 120 in Fig. 3), to receive a detach control signal (i.e., switch controlling signal from converting circuit 310 to switch 330 in Fig. 3) to cause said apparatus (i.e., USB converter) to enter a logically detached state (See col. 6, lines 27-30 and 50-67; i.e., in fact, even if said apparatus is physically connected (i.e., physically attached), the open switch (i.e., no voltage is supplied to D+) makes said apparatus set said logically detached state); and a serial data bus wire (i.e., USB interface D+ of Fig. 3) of said serial data bus coupled to said second end of said first resistor (See Fig. 3). Huang does not teach said logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus.

Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13-29) is sent from a far end (i.e., from a corresponding peripheral module; See col. 3, lines 26-28) of a serial data bus (i.e., bus 14 of Fig. 3; See col. 2, lines 43-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have received a logically detaching control signal from a far end of a serial data bus, as disclosed by Rafferty, in said apparatus, as disclosed by Huang, for the advantage of simulating insertion and removal (i.e., logically attaching and detaching) of said apparatus (i.e., USB device) by a corresponding far end device (i.e., a corresponding peripheral device; See Rafferty, col. 1, lines 50-58).

Huang, as modified by Rafferty, does not teach a wake-up signal wire separate from said data transmission wires of said serial data bus to send a wake-up signal from said near end of said serial data bus to said far end of said serial data bus to influence said detach control signal.

Pollard discloses a power management of a computer plug-in card having a remote data link 20 (Fig. 2), wherein a wake-up signal wire (i.e., status signal line 62 of Fig. 2) separate from a data transmission wires

of a data bus (i.e., data bus with power source line 36 through connectors 26, 28 in Fig. 2) to send a wake-up signal (i.e., 'link operable' signal 58 in Fig. 2) from a near end of said data bus (i.e., side of switch 46 in Fig. 2) to a far end of said data bus (i.e., side of host computer in Fig. 2) to influence a detach control signal (i.e., command output 52 of Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said wake-up signal wire, as disclosed by Pollard, in said apparatus, as disclosed by Huang, as modified by Rafferty, so as said switch (i.e., power connect switch) to operate responsive to said wake-up signal (i.e., status signal) indicating the operability of said near end of said data bus (i.e., a status monitor indicative of the operability of the remote data link capability) from said near end (i.e., power-consuming elements on the card) to said far end (i.e., power source in the computer), which is disclosed at Pollard, col. 2, lines 43-48.

Huang, as modified by Rafferty and Pollard, teaches said method step of influencing said detach control signal (i.e., switch controlling signal from converting circuit 310 to switch 330 in Fig. 3; Huang) with said wake-up signal (i.e., 'link operable' signal 58 in Fig. 2; Pollard) sent on said wake-up signal wire (i.e., status signal line 62 of Fig. 2; Pollard) separate from said data transmission wires (i.e., data lines D+ and D- in Fig. 3; Huang) of said serial data bus (i.e., USB in Fig. 3; Huang) from said near end of said serial data bus (i.e., a side of switch) to said far end of said serial data bus (i.e., the other side of switch).

Referring to claim 9, Huang discloses said switch may apply said bias voltage to said first end of said first resistor responsively to a detach control signal (i.e., switch controlling signal from converting circuit 310 in Fig. 3) on said detach control signal wire (See col.6, lines 23-27).

Referring to claim 11, Huang discloses said serial data bus carries universal serial bus data (i.e., USB interface D+ of Fig. 3).

Referring to claim 15, Huang discloses an apparatus (i.e., USB converter 120 of Fig. 3), comprising: means for providing a first resistor with a first end and a second end (i.e., pull-up resistor 340

of Fig. 3) coupled to a switch (i.e., switch 330 of Fig. 3) and said second end coupled to a serial data bus wire (i.e., USB interface D+ of Fig. 3) at a near end of a serial data bus (i.e., detach control signal wire from converting circuit 310 to switch 330 and data lines D+ and D-, which are located within USB converter 120 in Fig. 3); means for controlling said switch with a detach control signal (i.e., switch controlling signal from converting circuit 310 in Fig. 3) on a detach control signal wire (i.e., detach control signal wire) separate from data transmission wires (i.e., data lines D+ and D-) of said serial data bus (i.e., detach control signal wire and data lines D+, D-) to cause said apparatus (USB converter 120 of Fig. 3) to enter a logically detached state (See col. 6, lines 27-30 and 50-67; i.e., in fact, even if said apparatus is physically connected (i.e., physically attached), the open switch (e.g., no voltage is supplied to D+) makes said apparatus set said logically detached state); and means for switching a biasing voltage from said resistor utilizing said switch (See col. 6, lines 23-27).

Huang does not teach said logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus.

Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13-29) is sent from a far end (i.e., from a corresponding peripheral module; See col. 3, lines 26-28) of a serial data bus (i.e., bus 14 of Fig. 3; See col. 2, lines 43-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have received a logically detaching control signal from a far end of a serial data bus, as disclosed by Rafferty, in said apparatus, as disclosed by Huang, for the advantage of simulating insertion and removal (i.e., logically attaching and detaching) of said apparatus (i.e., USB device) by a corresponding far end device (i.e., a corresponding peripheral device; See Rafferty, col. 1, lines 50-58).

Huang, as modified by Rafferty, does not teach means for influencing said detach control signal with a wake-up signal sent on a wake-up signal wire separate from said data transmission wires of said serial data bus from said near end of said serial data bus to said far end of said serial data bus.

Pollard discloses a power management of a computer plug-in card having a remote data link 20 (Fig. 2), wherein means for influencing a detach control signal (i.e., command output 52 of Fig. 2) with a wake-up signal (i.e., 'link operable' signal 58 in Fig. 2) sent on a wake-up signal wire (i.e., status signal line 62 of Fig. 2) separate from a data transmission wires of a data bus (i.e., data bus with power source line 36 through connectors 26, 28 in Fig. 2) from a near end of said data bus (i.e., side of switch 46 in Fig. 2) to a far end of said data bus (i.e., side of host computer in Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said wake-up signal wire, as disclosed by Pollard, in said apparatus, as disclosed by Huang, as modified by Rafferty, so as said switch (i.e., power connect switch) to operate responsive to said wake-up signal (i.e., status signal) indicating the operability of said near end of said data bus (i.e., a status monitor indicative of the operability of the remote data link capability) from said near end (i.e., power-consuming elements on the card) to said far end (i.e., power source in the computer), which is disclosed at Pollard, col. 2, lines 43-48.

Huang, as modified by Rafferty and Pollard, teaches said method step of influencing said detach control signal (i.e., switch controlling signal from converting circuit 310 to switch 330 in Fig. 3; Huang) with said wake-up signal (i.e., 'link operable' signal 58 in Fig. 2; Pollard) sent on said wake-up signal wire (i.e., status signal line 62 of Fig. 2; Pollard) separate from said data transmission wires (i.e., data lines D+ and D- in Fig. 3; Huang) of said serial data bus (i.e., USB in Fig. 3; Huang) from said near end of said serial data bus (i.e., a side of switch) to said far end of said serial data bus (i.e., the other side of switch).

Referring to claim 17, Huang discloses said apparatus of claim 15, further comprising means for detecting said switching of said biasing voltage (See col. 6, lines 30-35).

Referring to claim 19, Huang discloses a system, comprising: a serial data bus (i.e., USB interface in Fig. 1 and 2) with a near end (i.e., side of USB converter 120 in Fig. 1) and a far end (i.e., side of computer system 110 in Fig. 1); a first circuit (i.e., USB converter 120 of Fig. 1), coupled to said near end (See Fig. 1), including a first resistor with a first end and a second end (i.e., pull-up resistor 340 of Fig. 3), a switch (i.e., switch 330 of Fig. 3) coupled to said first end of said first resistor and to a bias voltage (i.e., 3.3V in Fig. 3), a serial data bus wire (i.e., USB interface D+ of Fig. 3) of said serial data bus coupled to said second end of said first resistor (See Fig. 3), a detach control signal wire (i.e., switch controlling signal arrow from converting circuit 310 to switch 330 in Fig. 3) separate from data transmission wires (i.e., data lines D+ and D-) of said serial data bus (i.e., detach control signal wire and data lines D+, D-) coupled to said switch to receive a detach control signal (i.e., switch controlling signal) to cause said first circuit (i.e., USB converter) to enter a logically detached state (See col. 6, lines 27-30 and 50-67; i.e., in fact, even if said apparatus is physically connected (i.e., physically attached), the open switch (i.e., no voltage is supplied to D+) makes said first circuit set said logically detached state); and a second circuit (computer system 110 of Fig. 1), coupled to said far end (See Fig. 1).

Huang does not teach said logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus to said near end of said serial data bus.

Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13-29) is sent from a far end (i.e., from a corresponding peripheral module) of a serial data bus (i.e., bus 14 of Fig. 3; See col. 2, lines 43-45) to a near end (i.e., downstream module 16 of Fig. 4) of said serial data bus (See col. 3, lines 26-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have received a logically detaching control signal from a far end of a serial data bus, as disclosed by Rafferty, in said first circuit, as disclosed by Huang, for the advantage of simulating insertion and

removal (i.e., logically attaching and detaching) of said apparatus (i.e., USB device) by a corresponding far end device (i.e., a corresponding peripheral device; See Rafferty, col. 1, lines 50-58).

Huang, as modified by Rafferty, does not teach a wake-up control signal wire separate from said data transmission wires of said serial data bus to send a wake-up signal from said near end of said serial data bus to said far end of said serial data bus; and said second circuit to send said detach control signal responsive to said wake-up signal.

Pollard discloses a power management of a computer plug-in card having a remote data link 20 (Fig. 2), wherein a wake-up control signal wire (i.e., status signal line 62 of Fig. 2) separate from a data transmission wires of a data bus (i.e., data bus with power source line 36 through connectors 26, 28 in Fig. 2) to send a wake-up signal (i.e., 'link operable' signal 58 in Fig. 2) from a near end of said data bus (i.e., side of switch 46 in Fig. 2) to a far end of said data bus (i.e., side of host computer in Fig. 2); and a second circuit (i.e., power source 24 in the computer of Fig. 2) to send a detach control signal (i.e., command output 52 of Fig. 2) responsive to said wake-up signal (i.e., 'link operable' signal from plug-in card 30 of Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said wake-up signal wire, as disclosed by Pollard, in said apparatus, as disclosed by Huang, as modified by Rafferty, so as said switch (i.e., power connect switch) to operate responsive to said wake-up signal (i.e., status signal) indicating the operability of said near end of said data bus (i.e., a status monitor indicative of the operability of the remote data link capability) from said near end (i.e., power-consuming elements on the card) to said far end (i.e., power source in the computer), which is disclosed at Pollard, col. 2, lines 43-48.

Huang, as modified by Rafferty and Pollard, teaches said method step of influencing said detach control signal (i.e., switch controlling signal from converting circuit 310 to switch 330 in Fig. 3; Huang) with said wake-up signal (i.e., 'link operable' signal 58 in Fig. 2; Pollard) sent on said wake-up signal wire (i.e.,

status signal line 62 of Fig. 2; Pollard) separate from said data transmission wires (i.e., data lines D+ and D- in Fig. 3; Huang) of said serial data bus (i.e., USB in Fig. 3; Huang) from said near end of said serial data bus (i.e., a side of switch) to said far end of said serial data bus (i.e., the other side of switch).

Referring to claim 20, Huang discloses said switch (switch 330 of Fig. 3) may apply said bias voltage (3.3V in Fig. 3) to said first end of said first resistor responsively to said detach control signal (switch controlling signal from converting circuit 310 in Fig. 3). Refer to col.6, lines 23-27.

Referring to claims 7, 10, 18 and 21, Huang discloses said detach control signal (i.e., switch controlling signal) is asserted (i.e., state of switch controlling signal which causes switch 330 to be closed) when said wake-up signal (i.e., converted signal from the signals transferred between non-PnP interface and USB interface) is de-asserted (i.e., state of the converted signal which ultimately causes switch 330 to be closed).

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang [US 6,131,134] in view of Rafferty [US 6,141,719 A] and Pollard [US 5,754,870 A] as applied to claims 1, 3-5, 7-11, 15 and 17-21 above, and further in view of Decuir [US 5,781,028].

Referring to claim 12, Huang, as modified by Rafferty and Pollard, discloses all the limitations of claim 12 except that does not teach said serial data bus carries IEEE-1394 bus data.
Decuir teaches a conventional bi-directional transmission line using an IEEE 1394 standard (Fig. 4), wherein said serial data bus (i.e., transmission line 51 of Fig. 4) carries IEEE-1394 bus data (See col. 2, lines 23-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said serial data bus wire, as disclosed by Decuir, to said serial data bus wire of said apparatus, as disclosed by Huang, as modified by Rafferty and Pollard, for the advantage of a high speed of data transmission, which is well know to one of ordinary skill in the art at the time the invention was made.

5. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang [US 6,131,134] in view of Rafferty [US 6,141,719 A] and Pollard [US 5,754,870 A] as applied to claim 1, 3-5, 7-11, 15 and 17-21 above, and further in view of Takasu [JP 407058800 A].

Referring to claim 13, Huang, as modified by Rafferty and Pollard, discloses all the limitations of claim 13 except that does not teach a second resistor with a first end and a second end.

Takasu teaches a second resistor (i.e., terminating register R_2 of Fig. 1) with a first end and a second end, said first end coupled to said serial data bus wire (i.e., transmission line 9 of Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said second resistor, as disclosed by Takasu, in said apparatus, as disclosed by Huang, as modified by Rafferty and Pollard, so as to provide effective termination on said bus, which is well know to one of ordinary skill in the art at the time the invention was made.

Referring to claim 14, Takasu discloses said second end of said second resistor is coupled to signal ground (i.e., R_2 of Fig. 1 as a pull-down resistor; See col. 4, lines 30-31).

Response to Arguments

6. Applicant's arguments filed on 30th of March 2004 have been fully considered but they are not persuasive.

In response to the Applicant's arguments with respect to "Claim 1 now recites in pertinent part ... The sketch shows a resistor R_{pu} and a pair of switch 24, 26 coupled to a near end of serial data bus (A), whose corresponding far side is in 'downstream USB device 22'. The switches have control signals 'LS select' and 'HS select'. However, these control signals are not sent from the far side of serial data bus (A). ... Applicant submits that the controlling signal coming from peripheral module 12 to the switches 24, 26 of downstream module 16 does not come from the far end of serial data bus (A) between downstream module 16 and downstream USB device 22, but rather instead from the far end of a second data bus 14. As the claim recites 'said serial data bus', the controlling signal must come from the far end of the same

serial data bus that is coupled to the resistor and switch. In the case of Rafferty, it does not. The resistor and switch are coupled to the near end of one serial data bus: the controlling signal comes from a different data bus. ..." on the Response page 7, line 13 through page 9, line 15, the Examiner believes that the Applicant misinterprets the claim rejection under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Rafferty and Pollard.

The Applicant essentially argues that Rafferty doesn't teach the above argued elements, i.e., the detach control signal comes from the far end of the serial data bus that is coupled to the resistor and switch.

In fact, Huang teaches a near end of a serial data bus (i.e., data lines D+ and D- in Fig. 3) that is coupled to resistor 340 and switch 330 in Fig. 3; a far end of said serial data bus (i.e., the opposite end of said serial data bus); and detach control signal for controlling (i.e., opening or closing) said switch.

The Examiner admits that Huang does not teach said detach control signal coming from said far end of said serial data bus to said near end of said serial data bus. In other words, Huang's deficiency is that said detach control signal does not come from said far end of said serial data bus.

Therefore, the Examiner brought Rafferty, and trying to show an obviousness of the claimed invention, such that a detach control signal (i.e., switch controlling signal) being sent from a far end (i.e., from a corresponding peripheral module) of a serial data bus (i.e., I^2C bus 14 of Fig. 3), which has been admitted by the Applicant on the Response, page 9, line 3.

In spite of the above reasonable obviousness of the claimed invention (See paragraph 3 of the instant Office Action, claim rejection under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Rafferty and Pollard), the Applicant merely alleges that Rafferty does not teach that controlling signal coming from peripheral module 12 to the switches 24, 26 of downstream module 16 does not come from the far end of serial data bus (A) between downstream module 16 and downstream USB device 22. The Examiner believes that the Applicant misinterprets the claim rejection.

Actually, Rafferty teaches two different serial buses, which are USB bus between Downstream module 16 and USB device 22, and I^2C bus 14 between Downstream module 16 and Peripheral module 12 in Fig. 3. The Examiner brought Rafferty for showing the obviousness of the claimed invention, such that Rafferty suggests the subject matter "detach control signal" (i.e., switch controlling signal), and said switch controlling signal (i.e., detach control signal) coming form a far end of a serial data bus (i.e., I^2C bus 14 of Fig. 3), which is admitted by the Applicant.

The Examiner clearly states that the subject matter "serial data bus" is obviously suggested by the bus 14 in Fig. 3 (i.e., I^2C bus; See Office Action mailed on 30th of December 2003, page 3, lines 9-10), but the Applicant intentionally ignores the proper combination (i.e., element mapping) of the claim rejection, i.e., the subject matter "serial data bus" in the claimed invention is mapped to the subject matter "the bus 14 in Fig. 3" in Rafferty. Instead, the Applicant asserts that the subject matter "serial data bus" in the claimed invention should be the serial bus (A) between downstream module 16 and downstream USB device 22 in Fig. 3 by Rafferty because the subject matter "serial data bus" is coupled to the subject matters "resistor" and "switch".

However, Huang clearly teaches the subject matter "serial data bus" is coupled to the subject matters "resistor" and "switch", and further teaches the subject matters "near end" and "far end" on the subject matter "serial data bus", and Rafferty is suggesting the limitation "a detach control signal coming from a far end of a serial data bus". And, the Examiner has clearly pointed out rationale for appropriate combination of the references. Thus, the Applicant's arguments on this point are not persuasive.

In response to the Applicant's arguments with respect to Claims 8, 15 and 19 rejection on the Response pages 9-14, the Applicant's arguments on this point are not persuasive since the above Examiner's response.

In response to the Applicant's arguments with respect to "In the Office Action, at paragraph 7, it is stated that ...Applicant instead has argued that certain claim elements and limitations are not disclosed

in any of Huang, Rafferty, and Pollard. To establish a prima facie case of obviousness, case law requires three criteria. ... Applicant submits that he has demonstrated that all the claim limitations are not disclosed in any of the combined references Huang, Rafferty, and Pollard. ... Applicant respectfully submits that there has been no rationale for combining the cited references. ..." on the Response pages 16-17, the Examiner respectfully disagrees.

In contrary to the Applicant's statement, all the claimed elements and limitations are suggested by Huang, Rafferty, and Pollard (See paragraph 3 of the instant Office Action). Further, the Applicant fails to point out what are the certain elements and limitations in the claimed invention, which has not been disclosed in any of Huang, Rafferty, and Pollard.

Furthermore, all the rejections under *35 USC §103(a)* in the prior and the instant Office Action established a *prima facie* case of obviousness meeting the three basic criteria of the M.P.E.P. 2143.03 (8th ed. 2001). And, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Moreover, contrary to the Applicant's mere allegation, such that no "suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combines reference teaching" has been presented in the Office Action, the Examiner has clearly pointed out rationale for appropriate combination of the references, such that the motivation for the combination of Huang and Rafferty has been stated in lines 11-15 of the instant Office Action, page 3, and the motivation for the combination of Huang, Rafferty and Pollard has been stated in lines 3-7 of the instant Office Action, page 4. Thus, the Applicant's arguments on this point are not persuasive.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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